# Timing Measurements for the SXFT system

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Edited 2-17-2006
Edited 4-5-2006 Text and measurements in blue was added on this data.
Edited 2-13-2007 Added Timing measurements from within Stereo Finder FPGA

Two setups: 1st setup had two dual fibers(20 ft.) between the Mezzanine boards. 2nd setup had the old production 6 fiber cable(4 fibers used) connected to the TX Mezzanine board and those four fibers were connected to the dual fibers using a dual feed through connector, the two dual fibers were connected to the RX Mezzanine board.

Diagram shows the where the measurements were taken at.
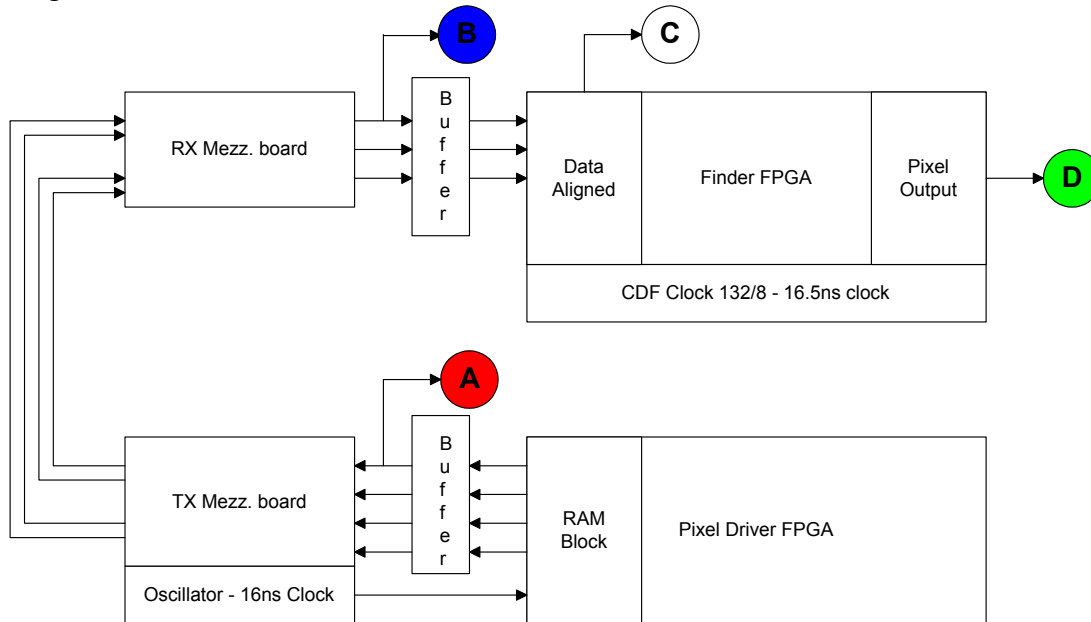
Time from Point A to Point B
1 : Time it takes to get from Finder FPGA output to SLAM board (1st setup)
138.08ns
2 : Time it takes to get from XTC transition board to Finder FPGA (2nd setup)
346.41ns   **Time with the new production Fiber was measured at 324ns(4/5/2006)**
 Time from Point A to Point C
3 : Time it takes to get from Finder FPGA output to Aligned data within the SLAM FPGA on the SLAM board(1st setup)(3 Fibers)
4 : Time it takes to get from XTC transition board to Aligned data within Finder FPGA (2nd setup) (3 Fibers)
461.42ns
3) Time from Point A to Point D
5 : Time it takes to get from XTC transition board to Pixel data out of the Finder FPGA(2nd setup)
923.09ns

6: Then if you add the Time 3 to Time 5 it should give us the time from XTC transition board to Aligned data within the SLAM FPGA.
1161.17ns

I would expect the measurements from the two setups to give the same delay through the Finder FPGA – as it did. The long fiber required an additional 16ns from Point B to Point C and I believe that was to align the data back up to the CDF clock.

For reference the red trace on the scope is the Data Valid signal being sent to the SERDES part. The Data Valid signal is aligned with the TX data.

The Blue signal is the same signal.

The yellow signal is within the Finder FPGA and tells when all three input FIFO's have data and the first slice of all three FIFOs are being read out aligned to CDF Clock/8.

The Green signal is referred to as Pixel Data valid and is 132ns wide or 8 cells worth of Pixel information. The 1st cells Pixel data is aligned with the rising edge of the green signal.

Setup 1: math
A to B = 138.08ns
B to C = 100ns
C to D = 461.07ns
B to D = 561.67 ns   **616ns to 648ns max. (625ns typ) v5r5 firmware**

! The 32ns variation is due to the TX board having a 16ns oscillator and the RX board having a separate 16ns oscillator. The Stereo Finder FPGA registers the RX data using the RX oscillator, converts the data to CDF_CLOCK/8 or 16.5ns and then the Pixel Driver section sends the data out of the FPGA using the TX oscillator. These measurements were made using one RX board, it may take another 16ns to align data from a second RX board which operates off it's own 16ns oscillator.

Setup 2: math
A to B = 346.41ns **Time with new production Fiber measured at 324ns (4/5/2006)**
B to C = 115.01ns * Extra 16ns to align data back to CDF clock
C to D = 461.07ns
B to D = 576.08 ns   **616ns to 648ns max. (625ns typ) v5r5 firmware**

Production 6 Fiber delay: 346.41 – 138.08 = 208.33 ns

Measured time from XTC transition to Aligned SLAM data:
Setup 2 delta value(6) of 923.09ns + Setup 1 delta value(2) of 238.08ns = 1161.17ns

*** These are measurements – the real system I suspect will be a little worse when data must become aligned from multiple crates and boards.

*** Also the latency within the SERDES parts and how oscillators and PLL within the FPGA are aligned with each other.

The following two pages contain the picture of the Screen on the oscilloscope for the two setups. The 1st picture on each of the pages shows all 4 traces and the 2nd and 3rd are cropped version of the same screen shot – the measurement was between waveforms A and B on the first screen shot, A and C on the second and A and C on the third screen shot.

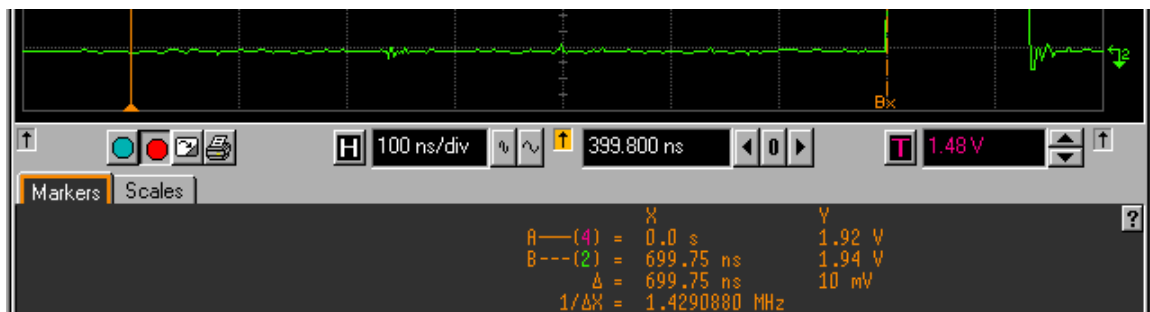SETUP 1 – Two dual fibers between TX and RX mezzanine boards
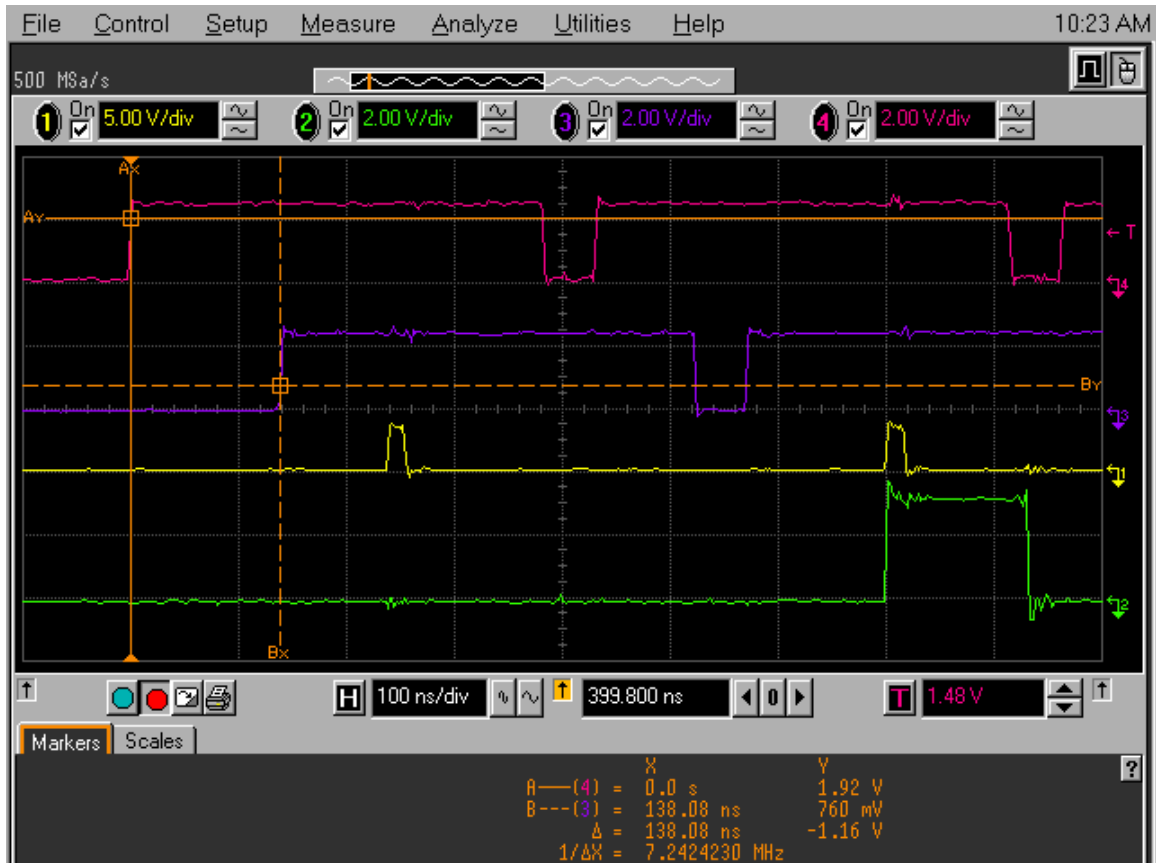
The delta value(1) of 138.08ns shows the time between Points A and B.
The following two pictures are cropped to just show the time measurement.
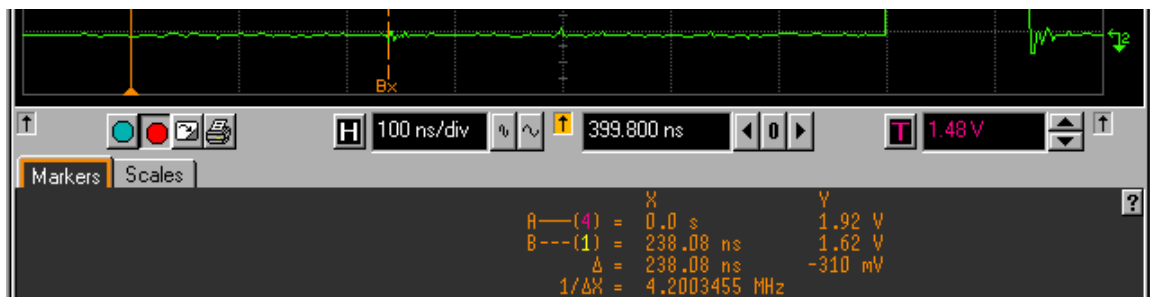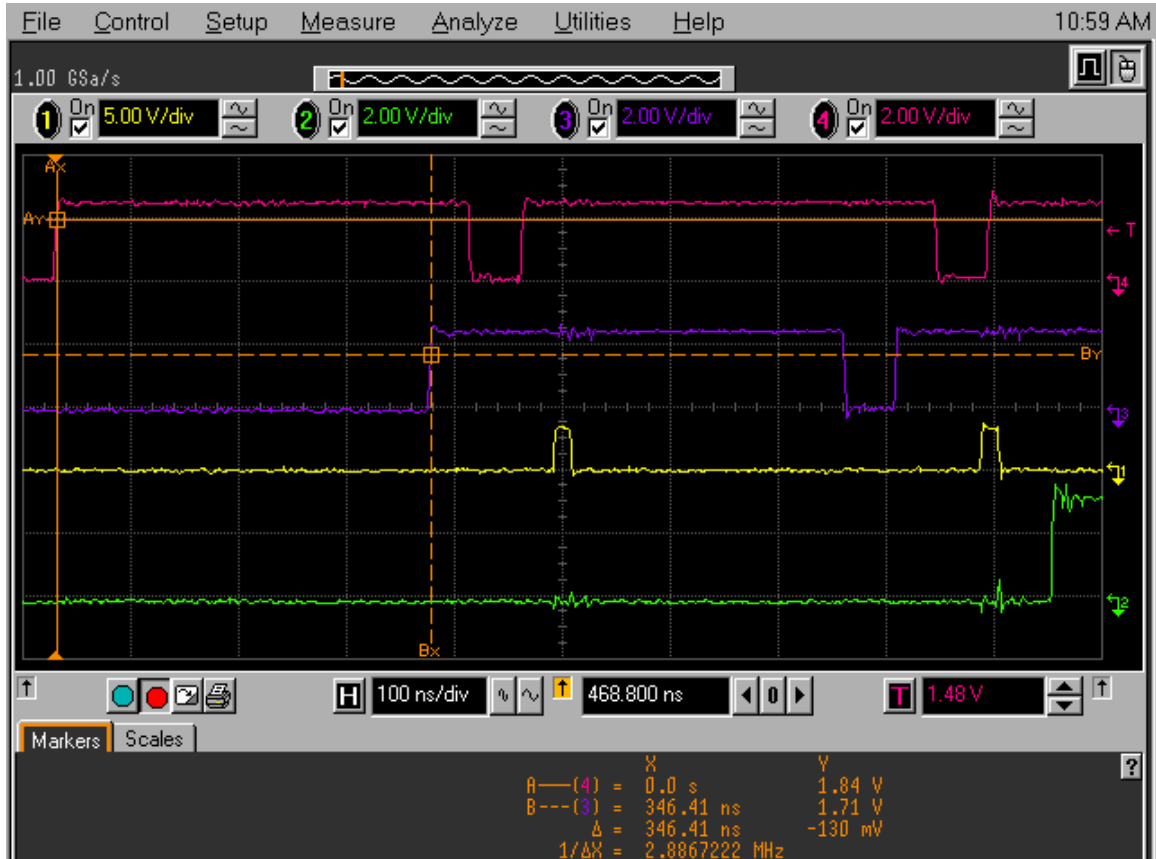

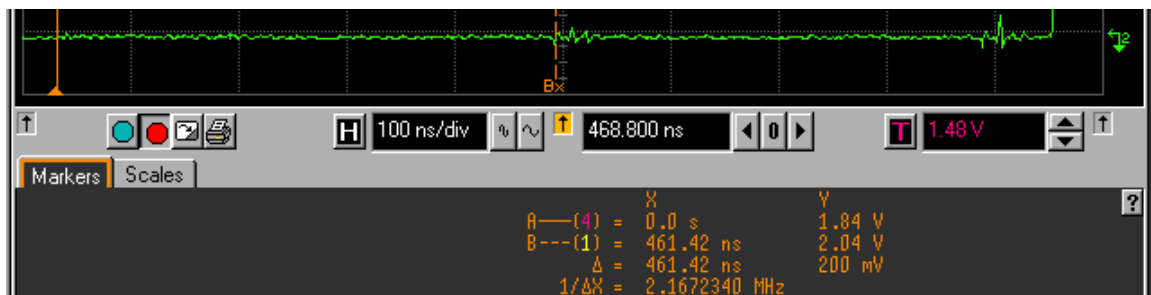The delta value(2) of 238.08ns shows the time between Points A and C.

The delta value(3) of 699.75ns shows the time between Points A and D.

SETUP 2 – OLD Production 6 fiber cable followed by two dual fibers between TX and RX mezzanine boards
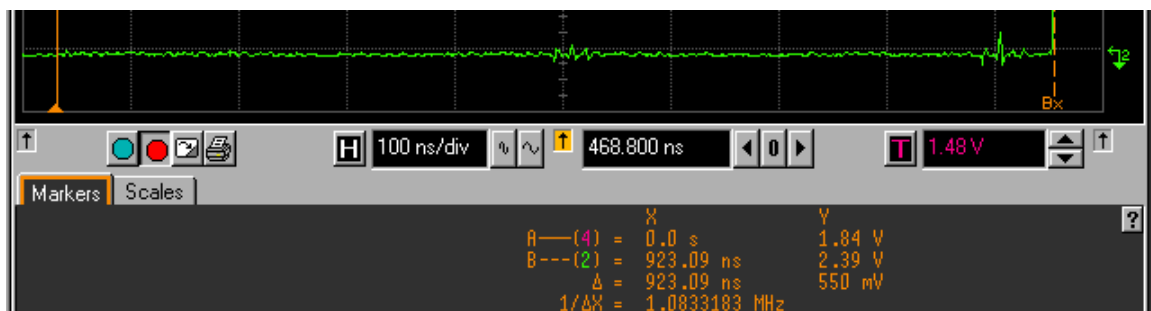

The delta value(4) of 346.41ns shows the time between Points A and B.
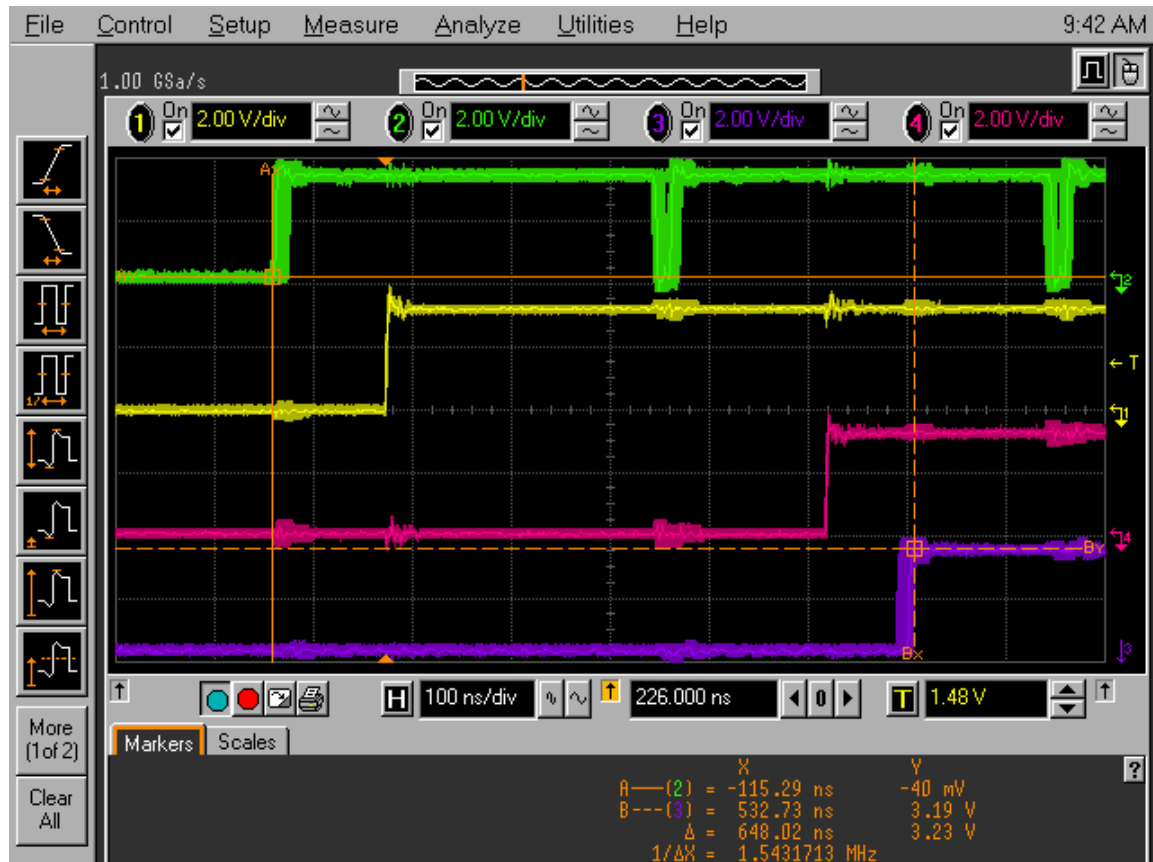The following two pictures are cropped to just show the time measurement.

The delta value(5) of 461.42ns shows the time between Points A and C.

The delta value(6) of 923.09ns shows the time between Points A and D.

Measurements and screen shots taken on 4/5/2006

Green = Data Valid that is output from the RX board(external FPGA).
Yellow = Data Aligned signal after Data is read out of the Alignment FIFOs.
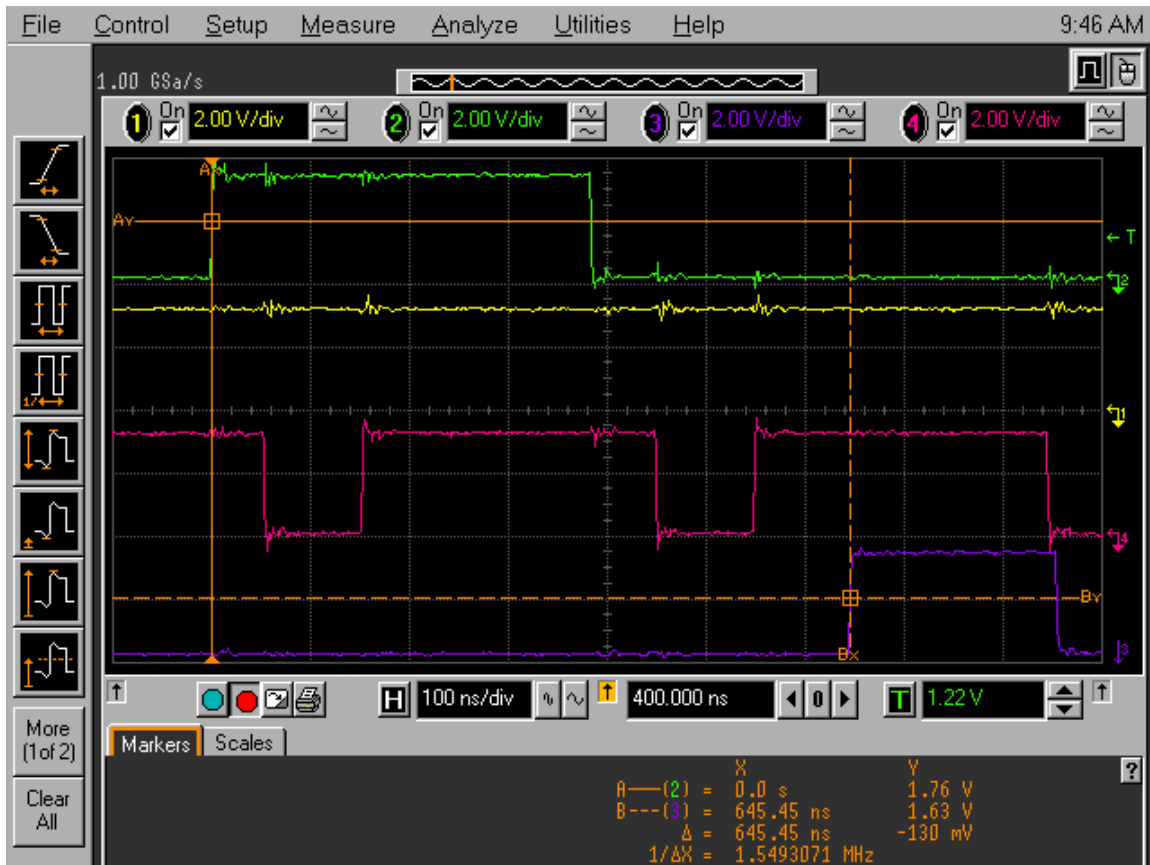Red = Data Valid going into Pixel Alignment section.
Purple = Data Valid signal going to the SLAM driver(external FPGA).
The trigger is from the yellow trace which is using the 16.5ns clock, the green and purple traces are signals that are being registered with independent 16ns clocks(smearing of the signals).
The scope was setup to do continuous trigger.

The delta time(648ns) shows the delay that is produced within the Finder FPGA for Alignment of the wire data, acquiring the whole event and then producing the segment information.
The Segment information that is produced is sent to the Slam Driver section of the PCB.
The segment information is already aligned to the clock used in the Slam Driver Section.

Green = Data signal from event that is output from the RX board(external FPGA).
Yellow = Data Aligned signal after Data is read out of the Alignment FIFOs.
Red = Data Valid going into Pixel Alignment section.
Purple = Data signal signal going to the SLAM driver(external FPGA).

The trigger is from the green trace.
The scope was setup to do a single trigger.

The delta time(645ns) shows the delay that is produced within the Finder FPGA for Alignment of the wire data, acquiring the whole event and then producing the segment information.
The Segment information that is produced is sent to the Slam Driver section of the PCB.
The segment information is already aligned to the clock used in the Slam Driver Section.

Some other time measurement taken:
From Output of RX board to Output of Alignment: 98>114ns (16ns)(B to C on drawings).
From Output of Alignment to the Output of Mask: 443ns
From Output of Mask to the input of SERDES for SLAM: 72ns>88ns (16ns)
From Input of SERDES for SLAM to Output of RX board using the production Fiber: 324ns.(A to B on drawings)

Block Diagram of Stereo Finder FPGA
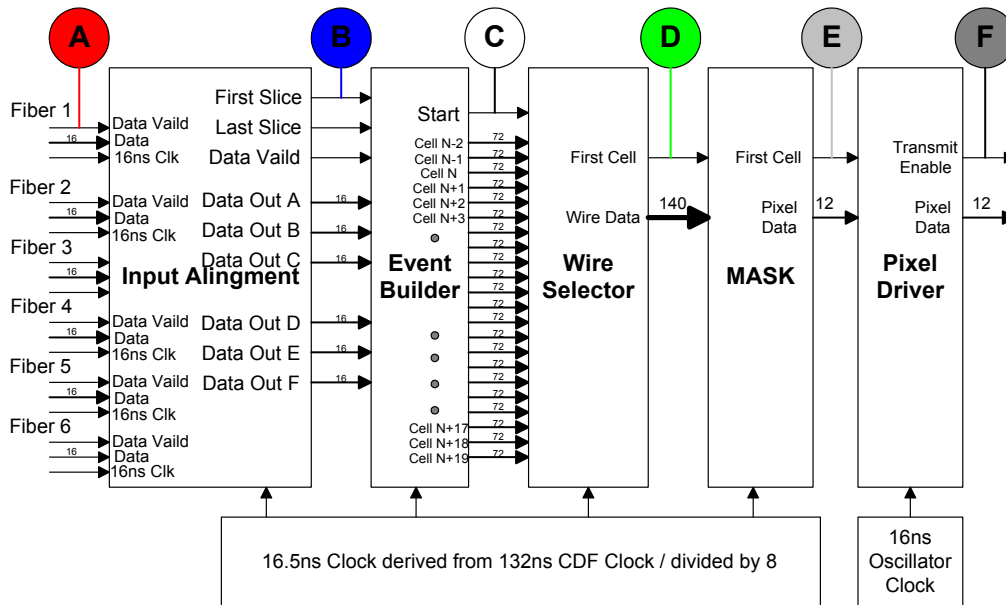
Time measurements were done by setting test points within the FPGA. The 6 fibers were driven using two TDC/XTC modules. The variation(Latency) between the 6 fibers was found to be about 34ns. This was found by measuring the difference between the data valid signal of the 6 different fibers. So another 14ns may need to be added to the total over all time to encompass the total latency that could occur due to SERDES part latency and the oscillators.

All the above points are measured at Test points on the board – the test points are connected to the FPGA pins.

A to B time = 144ns to 178ns

A to C time = 540ns to 574ns

A to D time = 557ns to 591ns

A to E time = 591ns to 625ns

A to F time = 694ns to 726ns

B to E time = 446ns * all blocks within this measurement operate from the 16.5ns clock so there is not a variation.